Amendment to the Drawings:

One new drawing sheet containing new Figs. 4 and 5 is enclosed. Figs. 4 and 5 have been added to illustrate the subject matter described in paragraphs [0018] and [0055] of applicants' published application (US 2007/0034880).

No new matter has been added.

Attachment: One New Sheet [Figs. 4 and 5]

REMARKS/ARGUMENTS

Status of Claims

Claims 1-5 and 7-15 are pending in this application with claim 1 being the only independent claim. Independent claim 1 has been amended to incorporate the additional features previously recited in claim 6, which has been cancelled without prejudice or disclaimer. No new matter has been added.

Reconsideration of the subject application is hereby requested.

Overview of the Office Action

The drawings have been objected to for allegedly failing to show each and every claim feature recited in the preamble of independent claim 1.

Claims 1-15 have been rejected under 35 U.S.C. § 103(a) as unpatentable over US 6,100,104 ("Haerle") in view of US 5,659,184 ("Tokunaga").

Claims 9-11 have been rejected under 35 U.S.C. § 103(a) as unpatentable over Haerle in view of Tokunaga, and further in view of US 6,110,277 ("Braun").

Remarks on Drawing Objection

In response to the drawing objection, applicants submit that the claim features at issue are already adequately shown in Fig. 1D and Fig. 2 (or Fig. 3), in conjunction with the descriptions in paragraphs [0036]-[0038] of applicants' published application (US 2007/0034880). More specifically, Fig. 1D depicts a growth stage of the optoelectronic semiconductor chips, where the mask material layer 11 is fully formed and contains a plurality of statistically distributed windows 2 of varying forms and opening areas (see para. [0036] of applicants' published application). Fig. 1D thus clearly illustrates "the production of a plurality of optoelectronic semiconductor chips," each of which has a plurality of structural elements with each structural

element comprising a semiconductor layer sequence that is subsequently formed as described below.

Figs. 2 and 3 show the subsequent production of the optoelectronic semiconductor chips, where a semiconductor layer sequence 8 is deposited selectively on a region of the growth surface 3 within each window 2 (see para. [0037] of applicants' published application). Although each of Figs. 2 and 3 shows only one semiconductor layer sequence 8, those skilled in the art will understand and appreciate that multiple semiconductor layer sequences 8 are being formed in the multiple windows 2 shown in Fig. 1D. Figs. 2 and 3 each represent and depict one of those multiple semiconductor layer sequences 8. Indeed, paragraph [0037] of applicants' published application expressly explains that "semiconductor layer sequences 8 are deposited selectively on regions of the growth surface 3 that lie within the windows 2."

In the subject application, each of these multiple semiconductor layer sequences 8 forms a structural element 12 (see para. [0038] of applicants' published application). Accordingly, each of Figs. 2 and 3 illustrates "the production of a plurality of optoelectronic semiconductor chips each having a plurality of structural elements with each structural element comprising a semiconductor layer sequence," as recited in independent claim 1.

Moreover, as mentioned above new Figs. 4 and 5, which further depict the claimed subject matter, have also now been added to the application.

In view of the foregoing, applicants submit that the drawing objection should be reconsidered and withdrawn.

Patentability of the Claimed Invention

A. Independent Claim 1

Independent claim 1 now recites "a layer of electrically conductive contact material that is transmissive to an electromagnetic radiation emitted by the active zone is applied to the

semiconductor layers, so that the semiconductor layers of a plurality of the structural elements are electrically conductively connected to one another by the contact material."

As perhaps best illustrated in new Figs. 4 and 5, a layer of electrically conductive contact material (7) is applied on the semiconductor layer sequences (8) and the mask material (1). This layer of electrically conductive contact material (7) electrically conductively connects the semiconductor layer sequences (8) of the multiple structural elements (12). (See, also, paras. [0018] and [0055] of applicants' published application.)

The above cited features of independent claim 1 are not taught by the combination of Haerle and Tokunaga, as discussed below.

(i)

The combination of Haerle and Tokunaga does not teach that "the semiconductor layers of a plurality of the structural elements are electrically conductively connected to one another by the contact material," as now expressly recited in independent claim 1.

Haerle teaches a method for fabricating a plurality of LED semiconductor bodies. According to Haerle, a mask layer 4 is formed on a substrate wafer 19 (see Fig. 1 and col. 6, ll. 38-40 of Haerle) and then photopatterned to form a plurality of windows 10 in the mask layer 4 (see Fig. 3 and col. 6, ll. 45-47). A semiconductor sequence 18, including a light-emitting layer 23, is epitaxially deposited in the windows 10, followed by the application of front-side contact metallization layers 15 to each semiconductor body to make contact with the LED structure 2 (see Figs. 4 and 5; col. 6, ll. 59; and col. 7, ll. 13-24). A contact metallization layer 15 is provided for each single structural element in each of the optoelectronic chips of Haerle (see Fig. 5, col. 7, ll. 22-24). The substrate wafer 3 of Haerle is then severed between the light-emitting diode structures 2 to obtain individual LED chips 100 (see Figs. 5 and 6 and col. 7, ll. 33-36).

In rejecting now-cancelled claim 6 (which contained the subject matter now recited in claim 1), the Examiner takes the position that Haerle's front-side contact metallization layers 15 electrically conductively connect the semiconductor layers of multiple structural elements (see page 6 of the Office Action). Applicants disagree.

As the Examiner acknowledges in the Office Action (see page 4 of the Office Action), Haerle does not disclose or suggest that any of its optoelectronic chips have a plurality of structural elements each containing a semiconductor layer sequence. Rather, each optoelectronic chip of Haerle has a single structural element containing a semiconductor layer sequence (see Figs. 6 and 7 and col. 7, ll. 33-36 of Haerle). Since no plural structural elements exist in any of Haerle's optoelectronic chips, Haerle cannot have a contact metallization layer 15 that electrically conductively connects multiple semiconductor layers of non-existent plural structural elements in its optoelectronic chip. In Haerle, the contact metallization layer 15 is provided for only the single structural element in each optoelectronic chip.

Therefore, Haerle does not disclose or suggest that "the semiconductor layers of a plurality of the structural elements are electrically conductively connected to one another by the contact material," as now expressly recited in independent claim 1.

Tokunaga is cited in the Office Action for allegedly teaching an optoelectronic semiconductor chip having a plurality of structural elements each containing a semiconductor layer sequence (see page 4 of the Office Action). Without admitting or disputing this interpretation of Tokunaga, applicants point out that Tokunaga does not remedy the above-discussed deficiencies of Haerle.

Tokunaga discloses a method for forming a III-V compound semiconductor device. For example, polycrystals of III-V compound semiconductor material are formed on a substrate 101 using a film 102 having windows (see Fig. 1L and col. 7, ll. 50-52 of Tokunaga). A III-V

compound is grown in areas of the windows in the film 102 (see Figs. 1D-1F). Afterwards, a metal electrode 108 is formed on the III-V compound to form the LED's as a one-dimensional array (see Figs. 1H-1J and 15G and col. 16, ll. 54-56). In Tokunaga's LED array, each LED has an individual electrode 1506 (see, e.g., Fig. 15G).

There is no teaching or suggestion in Tokunaga that any of its individual electrodes 1506 electrically conductively connect the LED's to one another in its LED array. Rather, the LED's in Tokunaga's LED array have individual electrodes 1506. Tokunaga, therefore, does not teach that "the semiconductor layers of a plurality of the structural elements are electrically conductively connected to one another by the contact material" as expressly recited in applicants' independent claim 1.

Tokunaga thus does not remedy the deficiencies of Haerle.

Accordingly, independent claim 1 is not obvious over the combination of Haerle and Tokunaga for at least the above reasons.

(ii)

The combination of Haerle and Tokunaga additionally does not teach or suggest that "a layer of electrically conductive contact material that is transmissive to an electromagnetic radiation emitted by the active zone is applied to the semiconductor layers," as now expressly recited in independent claim 1.

There is no disclosure or suggestion in Haerle that its contact metallization layers 15 are transmissive to light emitted by the light-emitting layer 23. Haerle is in fact silent concerning the material to be used to form the contact metallization layers 15. Haerle therefore does not teach or suggest that "a layer of electrically conductive contact material that is transmissive to an electromagnetic radiation emitted by the active zone is applied to the semiconductor layers," as now expressly recited in applicants' independent claim 1.

Tokunaga, moreover, does not remedy such deficiencies of Haerle.

Accordingly, independent claim 1 is not obvious over the combination of Haerle and Tokunaga for the above additional reasons.

In view of the foregoing, independent claim 1 is deemed to patentably distinguish over the cited combination of Haerle and Tokunaga. The 35 U.S.C. § 103(a) rejection of independent claim 1 should accordingly be reconsidered and withdrawn.

B. Dependent Claims 2-5 and 7-15

Claims 2-5 and 7-15 depend, directly or indirectly, from allowable independent claim 1 and thus are each deemed to be allowable therewith. In addition, dependent claims 2-5 and 7-15 each include features which serve to still further distinguish the claimed invention over the cited prior art.

Conclusion

In view of the foregoing, reconsideration, withdrawal of all rejections, and allowance of all pending claims are respectfully solicited.

Should the Examiner have any comments, questions, suggestions, or objections, the Examiner is respectfully requested to telephone the undersigned to facilitate an early resolution of any outstanding issues.

Respectfully submitted,
COHEN PONTANI LIEBERMAN & PAVANE LLP

By /Lance J. Lieberman/
Lance J. Lieberman
Reg. No. 28,437
551 Fifth Avenue, Suite 1210
New York, New York 10176
(212) 687-2770

Dated: March 1, 2010